third hard mask layer may be sequentially formed on the second insulation pattern **126***b* and the second electrode **132**.

[0223] The processes substantially the same as or similar to those illustrated with reference to FIGS. **5** to **14** may be performed again. However, a third hard mask may extend in a direction different from the direction of the first hard mask, and a fourth hard mask may extend in a direction different from the direction of the second hard mask. Particularly, the third hard mask may extend in the second direction, and the fourth hard mask may extend in the first direction. The upper structure **200***b* may include first spacers **228***a* and second spacers **228***b*. The first spacers **228***a* and second spacers **228***b* of the upper structure **200***b* may be formed of the same materials as the first spacers **128***a* and the second spacers **128***b* in the lower structure **200***a*. Alternatively, the first spacers **228***a* and second spacers **228***b* of the upper structure **200***b* may be formed of different materials than the first spacers **128***a* and the second spacers **128***b* in the lower structure **200***a*.

[0224] Thus, the second conductive line **205** may be formed on the second insulation pattern **126***b* and the second electrode **132**, and may extend in the second direction. The upper memory cell may be formed on the second conductive line **205**, and may include the second switching pattern **206***b*, the third electrode **208***b*, the third and fourth insulation patterns **226***a* and **226***b*, the second variable resistance pattern **230** and the fourth electrode **232**.

[0225] A third conductive layer may be formed on the fourth electrode **232** and the fourth insulation pattern **226***b*, and the third conductive layer may be patterned to form the third conductive line **234** extending in the first direction.

[0226] As described above, the semiconductor device including stacked memory cells at a plurality of levels may be manufactured. Also, failures of the semiconductor device due to the mis-alignment may decrease.

[0227] FIG. **28** is a block diagram illustrating a schematic construction of an information processing system in accordance with example embodiments.

[0228] Referring to FIG. **28**, an information processing system **500** may include a CPU **520**, a RAM **530**, a user interface **540**, a modem **550**, e.g., a baseband chipset, and at least one memory system **510**, which may be electrically connected to a system bus **505**. The memory system **510** may include a memory device **512** and a memory controller **511**. The memory device **512** may include one of the above-described variable resistance memory devices in accordance with example embodiments. Thus, large data processed by the CPU **520** or input from an external device may be stored in the memory device **512** with high stability. The memory controller **511** may have a construction capable of controlling the memory device **512**. The memory system **510** may serve as, e.g., a memory card or a solid state disk (SSD) by a combination of the memory device **512** and the memory controller **511**. When the information processing system **500** is a mobile device, a battery may be further provided for supplying a driving voltage of the information processing system **500**. The information processing system **500** may further include an application chipset, a camera image processor (CIS), a mobile DRAM, etc. The information processing system **500** may be used for mobile phones, MP3 players, and various appliances.

[0229] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and features of example embodiments of inventive concepts. Descriptions of features or aspects within each device or method according to example embodiments should typically be considered as available for other similar features or aspects in other devices or methods according to example embodiments. Accordingly, all such modifications are intended to be included within the scope of example embodiments of inventive concepts as defined in the claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures. Therefore, it is to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

1. A semiconductor device, comprising:

a substrate;

a plurality of first conductive lines on the substrate, the first conductive lines extending in a first direction;

a plurality of first structures on the first conductive lines, the first structures being spaced apart from each other, the first structures including a switching pattern and a first electrode sequentially stacked, and top surfaces of the switching pattern and the first electrode being substantially coplanar with each other;

a first insulation pattern on the substrate, the first insulation pattern extending in the first direction between the first structures to fill a space between the first structures in a second direction that is substantially perpendicular to the first direction, and the first insulation pattern having a first top surface that is higher than a top surface of the first structures;

a second insulation pattern on the substrate, the second insulation pattern extending in the second direction between the first structures to fill a space between the first structures in the first direction, and the second insulation pattern having a second top surface that is higher than a top surface of each of the first structures;

a variable resistance pattern on the first structures, the variable resistance pattern filling an opening defined by the first and second insulation patterns; and

a second electrode on the variable resistance pattern.

2. The semiconductor device of claim **1**, further comprising:

a first spacer on upper sidewalls of the first insulation pattern above the first structures; and a second spacer on upper sidewalls of the second insulation pattern above the first structures.

3. The semiconductor device of claim **2**, wherein a bottom surface of the variable resistance pattern is smaller than an area of the top surface of the first structures.

4-5. (canceled)

6. The semiconductor device of claim **1**, wherein a top surface of the variable resistance pattern is substantially coplanar with the first top surface of the first insulation pattern.

7. The semiconductor device of claim **1**, wherein the second electrode extends in the second direction.